REMARKS

In response to the Office Action mailed April 18, 2002, the Applicants respectfully request reconsideration.

Claims 1-9 were previously examined. By this amendment, Applicants add claims 10-18. As a result, claims 1-18 are pending for examination, of which claims 1 and 7 are independent.

1. Claims 1-6 and 10-14 Patentably Distinguish Over Aiello

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over U.S. Patent No. 5,382,837 (Aiello). Applicants respectfully traverse this rejection for at least the following reasons.

1.2 Discussion of Aiello

Aiello is directed to a switching circuit that connects a first circuit node to either a second or a third circuit node relative to a voltage potential on the third circuit node, and that controls the potential of an insulation region of an integrated circuit in relation to the potential of the substrate. (Col. 1, lines 7-12).

Aiello discloses several embodiments of the switching circuit (Figs. 1-6). Each embodiment includes a transistor T1 having an emitter connected to a ground potential, a collector connected to a an insulation region (Viso) and a base coupled to a power supply Vcc through a resistor R1. Each embodiment further includes a transistor T2 having an emitter connected to a substrate (Vsub) and a collector connected to Viso. (Figs. 1-6; Col. 3, line 37-col. 6, line 38). Some embodiments (Figs. 3-6) include a transistor T4 having an emitter connected to the base of T2, and some embodiments (Figs. 2, 4 and 6) include a transistor T3 having an emitter connected to Vsub, a collector coupled to Vcc through a resistor R1 and a base connected to the base of T2.

Aiello discloses that, when the potential of the substrate is greater than a reference potential (i.e., Vsub > zero), T2 is off and T1 is in saturation mode, thereby coupling the insulation region to the ground voltage. (Col. 3, line 59-col. 4, line 3; col. 4, lines 34-46) Thus, when the substrate potential is greater than the reference potential, the insulation region is coupled through a low impedance to the ground voltage.

Contrary to the assertions of the Office Action (Section 3, page 3, lines 3-6), Aiello does *not* disclose that the transistor T4 (Figs. 3-6) couples the insulation region (Viso) to the substrate (Vsub) *through a high impedance* when the substrate potential is greater than the reference potential. In contrast, when the substrate potential is less than a reference potential (i.e., Vsub<zero), T1 is off or reverse-biased and T2 is in saturation mode, thereby coupling the insulation region to the substrate. (Col. 4, lines 4-24, 47-54; Col.6, lines 14-17). Thus, when the substrate potential is less than the reference potential, the insulation region is coupled through a low impedance to the substrate.

1.2 Claim 1 is Not Rendered Obvious by Aiello

The Office Action asserts that it would have been obvious to a person of ordinary skill in the art to use Aiello's switching circuit as a protection structure against polarity inversion of a substrate potential. Applicants agree, as Applicants describe using Aiello's switching circuit as a protection structure in the specification. (Page 3, lines 6-19).

Claim 1 distinguishes from Aiello because Aiello fails to disclose or suggest an integrated circuit including, *inter alia*, a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, a bias circuit for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor with an emitter connected to the substrate and a base coupled to the isolation region **for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential**, as recited in claim 1. As set forth above, in contrast to claim 1, Aiello discloses coupling an insulation region to a substrate *through a low impedance* when a substrate potential is lower than the reference potential.

Therefore, for at least these reasons, claim 1 is not rendered obvious by Aiello. Accordingly, Applicant respectfully requests that the rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Aiello be withdrawn.

Claim 2-6 and 10-14, which each depend directly or indirectly from claim 1, are patentable over Aiello for at least the same reasons as set forth above with respect to claim 1. Accordingly, Applicant respectfully requests that the rejections of claims 2-6 under §103(a) be withdrawn.

2. Claims 7-9 and 15-18 Patentably Distinguish Over Aiello

Claims 7-9 stand rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over U.S. Patent No. 5,382,837 (Aiello et al.) Applicants respectfully traverse this rejection for at least the following reasons.

Claim 7 has been amended for clarification, not in response to any of the art of record, including Aiello.

Aiello fails to disclose or suggest a semiconductor device, comprising: a vertical power component having a terminal formed by a substrate of a first conductivity type; a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and a protection structure against polarity inversion of a substrate potential, comprising: a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit; a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and **means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential**, as recited in claim 7.

Therefore, for at least these reasons, claim 7 is not rendered obvious by Aiello. Accordingly, Applicant respectfully requests that the rejection of claim 7 under 35 U.S.C. §103(a) as being unpatentable over Aiello be withdrawn.

Claims 8, 9 and 15-18, which each depend directly or indirectly from claim 7, are patentable over Aiello for at least the same reasons as set forth above with respect to claim 7. Accordingly, Applicant respectfully requests that the rejections of claims 8 and 9 under §103(a) be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee

occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Antonio Torres, et al., Applicant(s)

By: _____

Daniel P. McLoughlin, Reg. No. 46,066
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Tel. No.: (617) 720-3500
Attorney for Applicant

Docket No.: S01022.80385.US
Date: January 22, 2003
xNDDx

MARKED-UP CLAIM

7. (Amended) A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and

[(iii) a second bipolar transistor having an emitter connected to the substrate and a base connected to the isolation region; and]

[(iv)] (iii) means for coupling [a high impedance means that couples] the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential.